

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1.    (Currently Amended) A digital processing system having a  
2    microprocessor, wherein the microprocessor comprises:

3        fetch circuitry for fetching instruction fetch packets from  
4    sequential memory address locations, wherein each fetch packet  
5    contains a first plurality of fixed length instructions, each  
6    instruction including an instruction type and a predetermined p-  
7    bit, said p-bit having a first digital state indicating a next  
8    instruction is to execute in parallel with said instruction and a  
9    second digital state indicating a next instruction is to execute in  
10   a cycle after said instruction;

11       a second plurality of functional units, each of the second  
12   plurality of functional units operable to execute a corresponding  
13   instruction in parallel with other functional units, and

14       dispatch circuitry connected to said fetch circuitry and said  
15   second plurality of functional units operable to

16       select an ~~execution~~ execute packet from ~~one or more~~ two fetch  
17   packets, wherein an execute packet varies in size and contains only  
18   a set of instructions that can be executed in parallel on the  
19   plurality of functional units, by scanning instructions from lower  
20   memory address locations to higher memory address locations  
21   beginning in a first fetch packet, adding an instruction to said  
22   execute packet when said p-bit of a prior instruction has said  
23   first digital state and continuing past an end of said first fetch  
24   packet to a beginning of a second fetch packet until said p-bit of  
25   an instruction has said second digital state, and

26       dispatch each instruction of said selected execute packet to a  
27   functional unit corresponding to said instruction type of said  
28   instruction.

Claims 2 and 3. (Canceled)

1 4. (Currently Amended) The digital processing system of  
2 Claim ~~2~~ 1, wherein the dispatch circuitry comprises:

3 a first latch to hold said first plurality of instructions of  
4 a first fetch packet, said first latch including a first plurality  
5 of sections, each section storing a corresponding one of said first  
6 plurality of instructions of said first fetch packet;

7 a second latch to hold said first plurality of instructions of  
8 a second fetch packet immediately following said first fetch  
9 packet, said second latch including a first plurality of sections,  
10 each section storing a corresponding one of said first plurality of  
11 instructions of said second fetch packet;

12 a first plurality of multiplexers, each multiplexer having a  
13 first input receiving an entire instruction from a predetermined  
14 ~~position~~ section of said first latch, a second input receiving an  
15 entire instruction from a corresponding ~~position~~ section of said  
16 second latch, a control input and an output, each multiplexer  
17 selecting at said output said entire instruction from said section  
18 of said first latch, said entire instruction from said section of  
19 said second latch, or no instruction, dependent upon said control  
20 input;

21 a dispatch control circuit connected to said first latch, said  
22 second latch, and said plurality of multiplexers, said dispatch  
23 control circuit receiving said predetermined p-bit from each  
24 instruction of said first latch and each instruction of said second  
25 latch for control of said plurality of multiplexers via said  
26 control inputs according to the execute packets determined by said  
27 p-bits; and

28 a cross point circuitry connected to said outputs of said  
29 plurality of multiplexers for dispatching said instructions at said

30 output of said multiplexers to a functional unit corresponding to  
31 said instruction type of each instruction.

Claims 5 and 6 (Canceled)

1        7. (Currently Amended) A method of operating a digital  
2 system having a microprocessor, wherein the microprocessor has a  
3 plurality of functional units for executing instructions in  
4 parallel, comprising the steps of:  
5        storing fixed length instructions at sequential memory address  
6 locations, each instruction including an instruction type and a  
7 predetermined p-bit, said p-bit having a first digital state  
8 indicating a next instruction is to execute in parallel with said  
9 instruction and a second digital state indicating a next  
10 instruction is to execute in a cycle after said instruction;  
11        fetching a sequence of instruction fetch packets, wherein each  
12 fetch packet contains a first plurality of instructions;  
13        scanning the p-bit of each instruction of each fetch packet  
14 from lowest memory address location in a first memory fetch packet  
15 to highest memory address location in a second immediately  
16 following fetch packet to determine an execute packet dependent on  
17 the p-bits;  
18        dispatching each instruction within the determined execute  
19 packet to one of a second plurality of execution units dependent  
20 upon an instruction type of the instruction.

Claim 8. (Canceled)

1        9. (Currently Amended) The method of Claim 7, wherein:  
2        said step of determining an execute packet boundary dependent  
3 upon the p-bits includes

4 storing a each instruction of said first fetch packet in  
5 a corresponding section of a first latch,  
6 storing a each instruction of said second fetch packet in  
7 a corresponding section a second latch,  
8 selecting an entire instruction from a predetermined  
9 section of said first latch, a—corresponding an entire  
10 instruction from a corresponding section of said second latch,  
11 or no instruction, dependent upon said p-bit from each  
12 instruction of stored in said first latch and each instruction  
13 of stored in said second latch.

Claims 10 and 11. (Canceled)